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Thermal diffusion: a simulation based study on shallow junction formation

U. Hashim[1*], N. Hamat N. H[2], Siti Fatimah[3], Tijjani Adam[4]

Nano Biochip Research Group, Institute of Nanoelectronics Engineering (INEE), Universiti Malaysia Perlis 01000 Kangar, Perlis, Malaysia

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Abstract

Ultra shallow junction fabrication in future ultra large scaled integrated (ULSI) technology is one of the difficult challenges in device manufacturing. Low energy ion implantation is the most widely used technique at present to form ultra shallow junction but research has been done to overcome its limitations such as crystal damage. In this research paper, thermal diffusion from spin-on dopant (SOD) into silicon has been studied in order to form shallow junction. This study was done by simulation using TSUPREM-4 from Synopsys Inc to determine the junction depth and the sheet resistance in order to fulfill the ITRS requirements. Ultra shallow junction which is defined to be less than 30 nm in depth has been obtained through this simulation using this easy and simple spin-on dopant technique. This economical spin-on dopant (SOD) technique has been proven as one promising method for shallow junction formation in future generations.

Keywords: Ultra shallow junction; Simulation; Thermal diffusion.
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1. Introduction

The functionality and performance of ICs are determined by the physical and electrical characteristics of the devices. In addition, the reliability and yield of ICs are related to the ability to control these characteristics precisely over a single wafer and across many wafers. A deeper understanding of the physical phenomena in ICs can only be provided by TCAD (Technology computer-aided design), which simulates the fabrication processes and electrical performance of transistors and interconnects using physical models [1]. TCAD provides a direct method to explore, optimize and control processes to achieve the desired properties of the key components.

Shallow junction formation is a hot topic in semiconductor industry and has been a very crucial process step in future CMOS generation [1, 4]. As transistors are made smaller, the junctions that form the source and drain regions of the transistor must be made shallower to improve the performance and provide sufficient breakdown characteristics. As technologists drive the limits of how shallow a junction can be fabricated, terminology has

*) For correspondence, E-mail: uda@unimap.edu.my

emerged which calls these aggressive processes as ultra shallow junctions (USJ). Ultra shallow junctions enable faster switching speeds with low leakage and low power requirements. Low energy ion implantation is the most popular technique used at present to fabricate ultra shallow junctions. But as an advanced technology, this technique unable to reduce its limitations such as damage to crystal and transiently enhanced diffusion upon annealing this damage [2,5]. Since crystal structure is damaged, there is an effect to junction depth [6, 7]. Many researchers have been done to improve the damages.

To overcome these limitations, dopant atoms from spin-on glasses (SOG) and in this case is called spin-on dopant (SOD) are used directly onto the silicon substrate before it was diffused by thermal diffusion [2]. Spin-on dopant technique is an easy and very simple to introduce dopant onto the substrate compared to the other methods such as ion implantation. At the diffusion temperature, the dopants are driven into the silicon. Thermal diffusion is generally applied in device fabrication and the furnace technology will continue to play an important role because of its maturity and economy. Rapid thermal process is also widely considered to be very attractive.

The trend in CMOS fabrication towards smaller gate lengths is a permanent challenge for silicon process simulation. In particular, since the miniaturization is intimately related to the fabrication of shallower p-n junctions, the demands for the simulation of the ultra shallow junctions are rapidly increasing.

2. Simulation Process

TSUPREM-4, a 2D process simulator from Synopsys Inc is used to model the whole process of junction formation for predicting the characteristics of the junction created by doping of silicon. The default model is applied in this simulation which actually using Fermi level diffusion model. The advantage of this default model is its fast execution. Default model only takes the normal diffusion of dopants into account and point defects are not directly represented.

TSUPREM-4 begins a simulation by defining a mesh elements and node points for the calculations. All TSUPREM-4 simulation files are two-dimensional, but the calculations are performed in one dimension as long as the structure has 1D uniformity. This simulation was considered the Y-direction only which the distance of the dopant diffusion into the wafer becomes our main concern. The Y-mesh was established fine enough to obtain appropriate results.

The structure is then initialized by defining the INITIALIZE statement determines the initial background doping level of the wafer. All relevant information including resistivity or doping level, impurity, material and crystalline orientation are specified. All the input data are corresponded to wafer specifications available in our laboratory.

There is no spin-on dopant (SOD) diffusion model is available in the TSUPREM-4 software. However, due to the similar diffusion behaviour of impurities from SOD and doped oxide technique, we have simulated the diffusion from SOD similarly to doped oxide model. The SOD is defined by depositing the oxide layer on top of silicon wafer with impurity specified in this layer. The DIFFUSION statement causes annealing to happen. It is common to specify multiple anneal steps in sequence in order to accurately model a specific furnace process [8]. The diffusion process is done in nitrogen ambient. The concern parameters are annealing temperature and time. Two different diffusion processes of practical interest, conventional furnace processing and rapid thermal processing are

simulated. In this paper, we investigated the diffusion of boron and phosphorus into n-type and p-type silicon substrates respectively.

Program output includes one and two dimensional plots of a specified quantities and extraction of parameters. The relevant parameters that are extracted from this process simulation are junction depth and sheet resistance.

3. Results and Discussion

The results will be discussed separately for boron and phosphorus.

3.1 Boron Diffusion

3.1.1 Conventional furnace

Table 1: Junction depth and sheet resistance vs temperature and time.

		Boron	
Temp (°C)	Time (minutes)	Xj (nm)	Rs (Ω/sq)
900	10	55.2	135
	20	91.2	127
	30	119.5	122
	60	192.2	110
950	10	148.6	116
	20	228.3	104
	30	291.7	97
	60	426.1	83

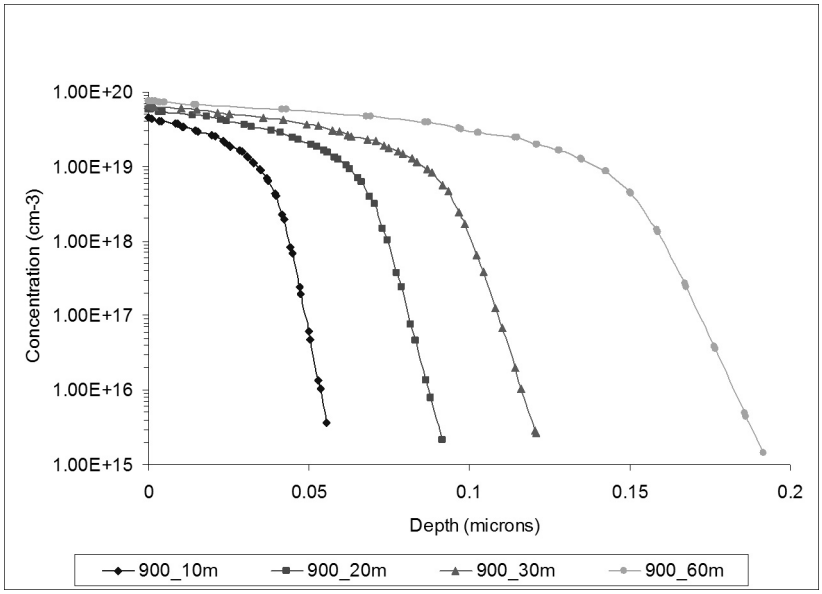

Fig. 1: Boron profile for furnace thermal diffusion done at 900°C.

Figure 1 shows the profiles of boron diffusion into silicon obtained from the simulation. The drive-in process was done at temperature of 900ºC in nitrogen ambient. Junction depths and sheet resistances are presented in Table 1. As shown in the table, the shallowest junction is 55.2 nm, obtained by diffusion at 900ºC for 10 minutes. Longer processing time and higher annealing temperature produces deeper junction as the dopant atoms acquire more energy to diffuse further into silicon substrate. This indicates that junction depth is strongly dependent on the processing temperature and time.

As seen in Figure 1, flat-topped profiles of boron are produced through this simulation. Willoughby [9] showed that increasing the surface concentration changed the profiles from complementary error function to a flat-top shaped. In this simulation, higher concentration of boron was used to match with boron SOD source in laboratory. Hence, the boron profiles in Figure 1 are distorted by high concentration effects.

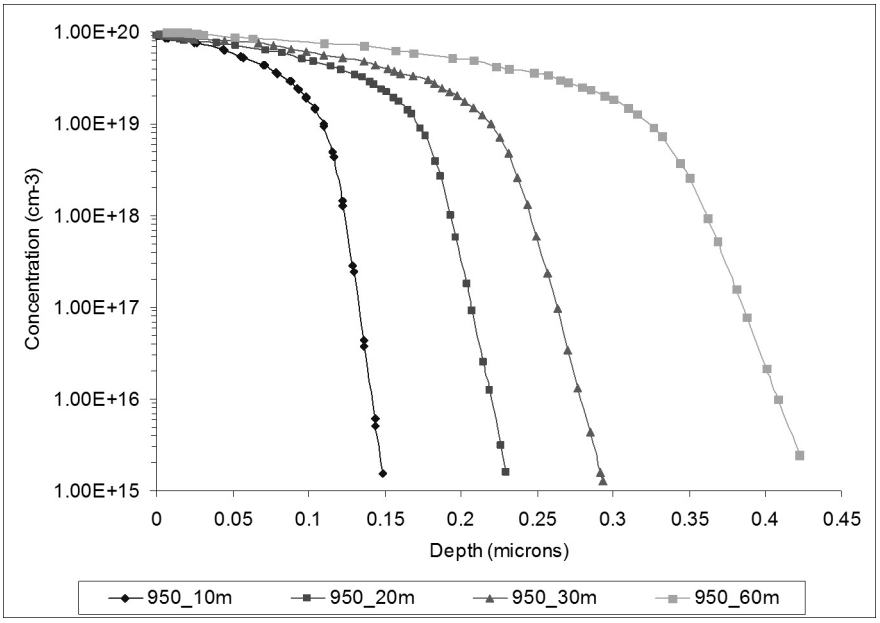

Fig. 2: Boron profile for furnace thermal diffusion done at 950°C.

Figure 2 shows the profiles of boron which the drive-in process was done at 950°C in nitrogen ambient. The shallowest junction produced at this temperature is 148.6 nm achieved from 10 minutes diffusion. This temperature results in deeper junction since the dopant obtains more energy to diffuse to the bottom position. At higher temperature, the dopants move faster into the substrates and will go deeper if the processing time is longer.

The sheet resistances are also reasonable and have met the ITRS requirements which require low sheet resistance. Figure 3 shows the dependence of sheet resistance on time and temperature. The sheet resistance gives the estimation of dopant activation level. As shown in Figure 3, the sheet resistances decrease sharply with an increase in processing temperature and time. This behavior is caused by the diffusion and subsequent activation of impurity atoms into silicon. The doping level is increased with the increasing of processing temperature. It is also noticed that sheet resistance variation for lower temperature diffusion is greater than higher temperature annealing.

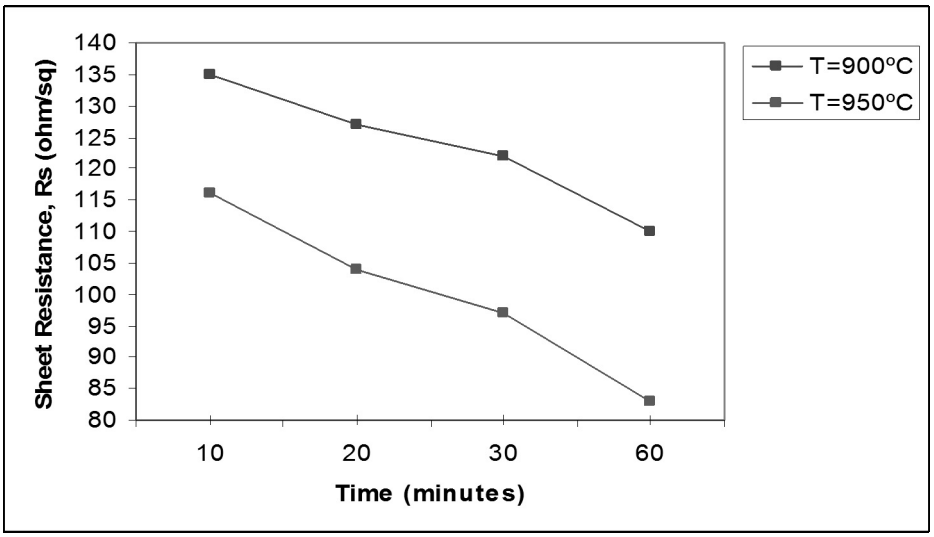

Fig. 3: Sheet resistance versus time.

3.1.2 Rapid thermal diffusion

Figure 4 and 5 show the simulated profiles for boron diffusion into silicon substrate by rapid thermal diffusion in nitrogen ambient. Table 2 represents the obtainable sheet resistances and junction depths through this simulation. According to this table, all the simulated junction depths are considered as ultra shallow junctions since the depths are less than 30 nm. The sheet resistances are also higher than the sheet resistances produced by furnace diffusion.

Table 2: Sheet resistances and junction depths for rapid thermal diffusion.

		Boron	
Temp (°C)	Time (seconds)	Xj (nm)	Rs (Ω/sq)
900	10	3.5	155
	20	5.8	154
	30	7.7	153
	60	11.7	151
950	10	9.3	152
	20	14.2	148
	30	18.6	144
	60	29.3	141

As expected, the doping level increases with increasing rapid thermal diffusion temperature. The doping level also increases with increasing rapid thermal diffusion duration. The diffusion of boron into the silicon is greater than that in the oxide so the peak boron concentration at the silicon surface decreases with processing time.

By rapid thermal diffusion, boron atoms diffuse to a shallower position if we compared to conventional furnace diffusion because of its processing time which the diffusion was done at shorter time which only done in seconds.

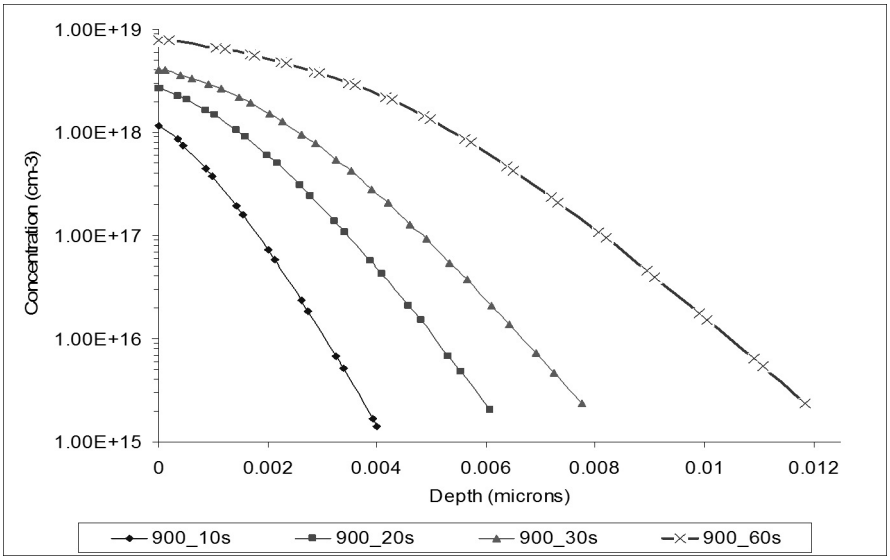

Fig. 4: Boron profile for rapid thermal diffusion done at 900°C.

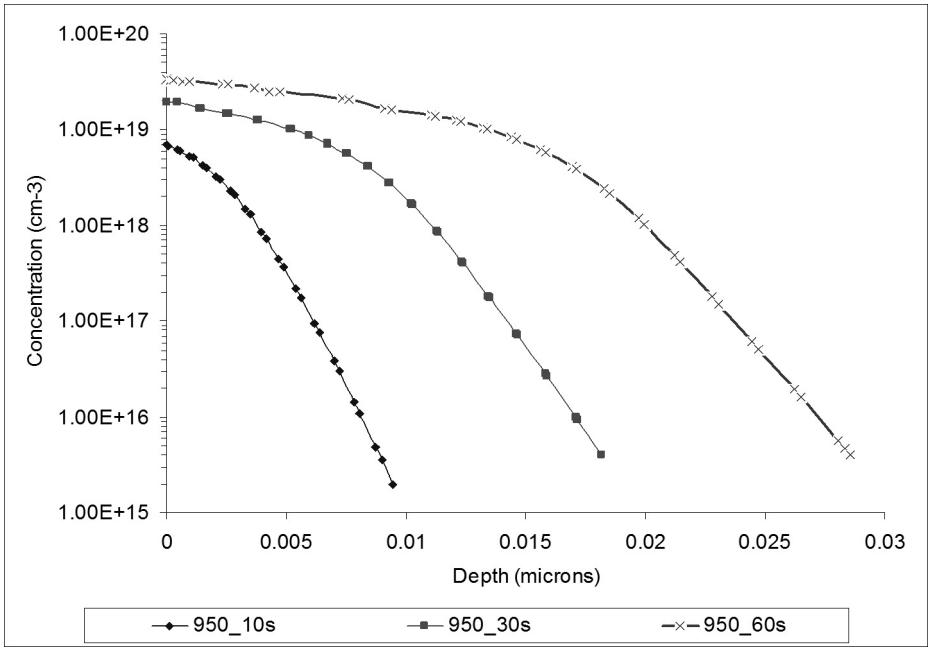

Fig. 5: Boron profile for rapid thermal diffusion done at 950°C.

3.2 Phosphorus Diffusion

Results of sheet resistances and junction depths obtained through this simulation are listed in Table 3 and 4.

Phosphorus has a high solid solubility in silicon. However, phosphorus diffusion under high concentration conditions in silicon is a complex phenomena and shows anomalous behavior as shown in Figure 6 to 9. Typical features of the phosphorus diffusion profile are a transition or kink region followed by a low concentration or tail region. On examination of the concentration versus depth curves of Figure 6 to 9, it is obvious that the results of phosphorus simulation follow the same basic trend as reported by the others. A high concentration region with a sharp drop-off near the surface followed by a kink and

finally a tail region are shown in the figures. A kink appears in the profile, the tail component of which penetrates deeper as the surface concentration is raised above 10^{19} cm^{-3}. This corresponds to an obvious increase in the diffusion coefficient of an order of magnitude, despite the fact that time and temperature is constant.

As shown in Table 3, the shallowest junction for phosphorus diffusion is 81.9 nm for conventional furnace annealing. This shallow junction was obtained by annealing at temperature of 900ºC for 10 minutes. But this junction cannot be considered as shallow junction since the depth is more than 50 nm. The sheet resistance for this junction is 189Ω/sq. This value is considered low. For rapid thermal diffusion, as assumed, the shallowest junction was obtained for structure simulated at 900ºC for 10 seconds with its value of 20.8 nm and sheet resistance of 496Ω/sq.

As boron diffusion, rapid thermal diffusion of phosphorus also produced ultra shallow junctions. But the depths are deeper than boron diffusion and likewise the lateral diffusion is also higher compare to boron [3].

Table 3: Sheet resistances and junction depths of phosphorus diffusion for conventional furnace.

Temp (°C)	Time (minutes)	Phosphorus	
		Xj (nm)	Rs (Ω/sq)
900	10	81.9	189
	20	101.7	178
	30	118.2	171
	60	151.7	161
950	10	131.4	168
	20	170.6	158
	30	199.3	155
	60	261.6	149

Table 4: Sheet resistances and junction depths of phosphorus diffusion for rapid thermal.

Temp (°C)	Time (seconds)	Phosphorus	
		Xj (nm)	Rs (Ω/sq)
900	10	20.8	496
	20	27.4	384
	30	31.2	343
	60	38.1	288
950	10	32.8	339
	20	40.6	280
	30	46.0	254
	60	57.9	219

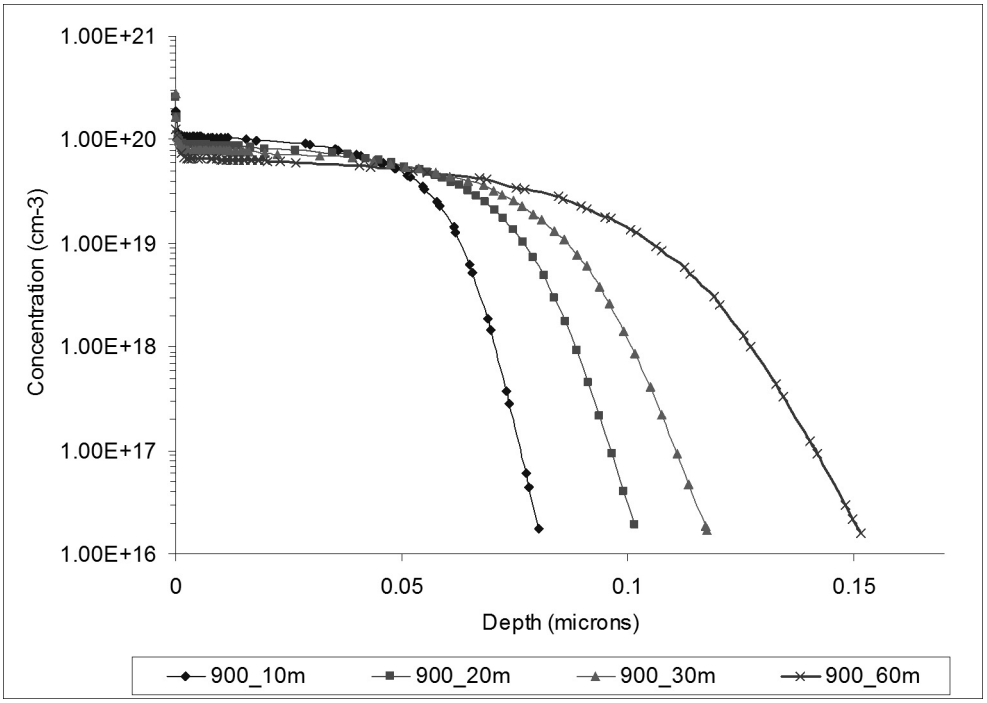

Fig. 6: Phosphorus profile for furnace thermal diffusion done at 900°C.

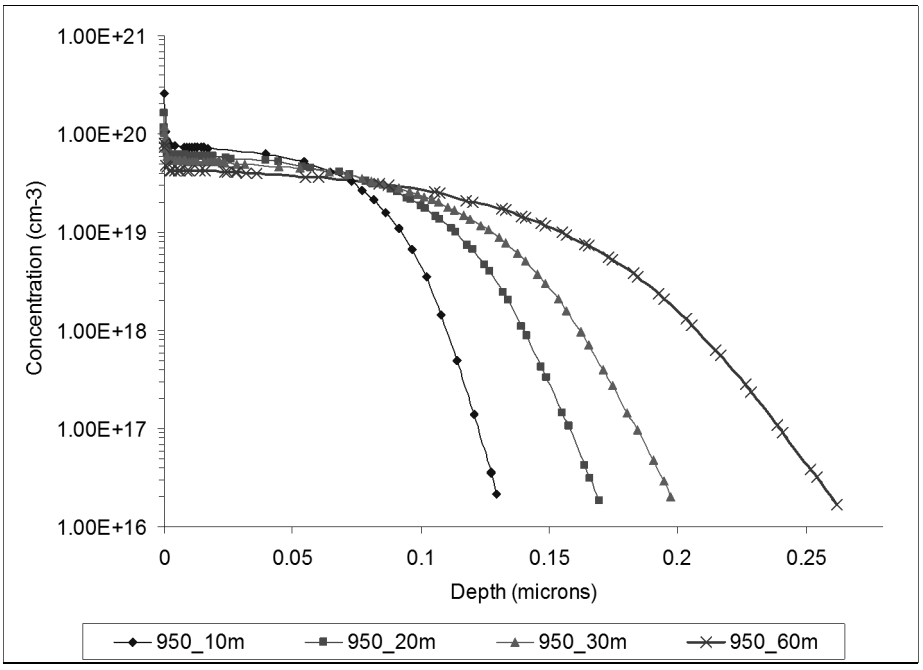

Fig.7: Phosphorus profile for furnace thermal diffusion done at 950°C.

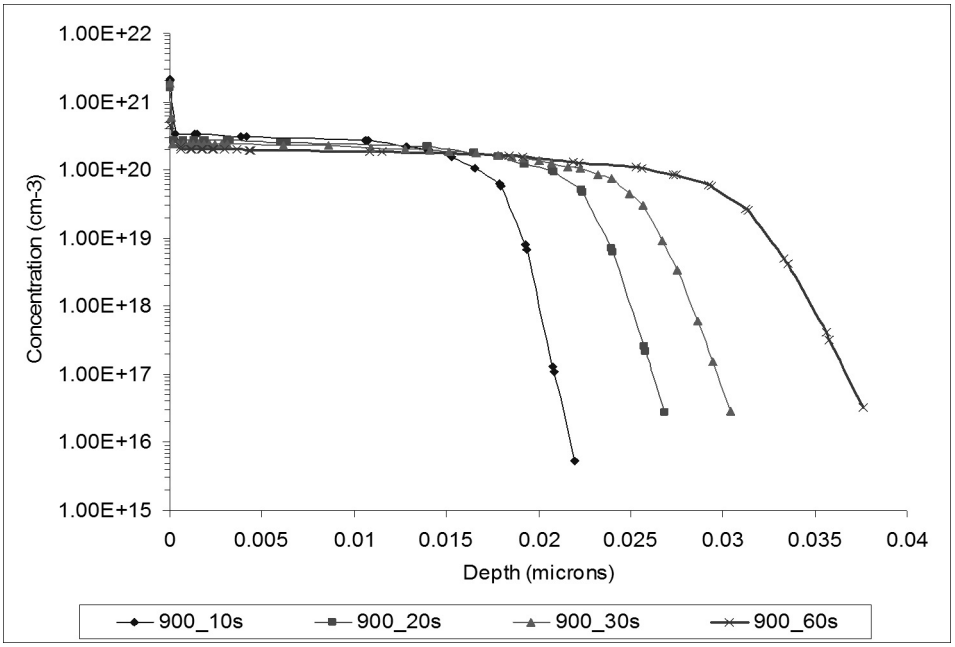

Fig. 8: Phosphorus profile for rapid thermal diffusion done at 900°C.

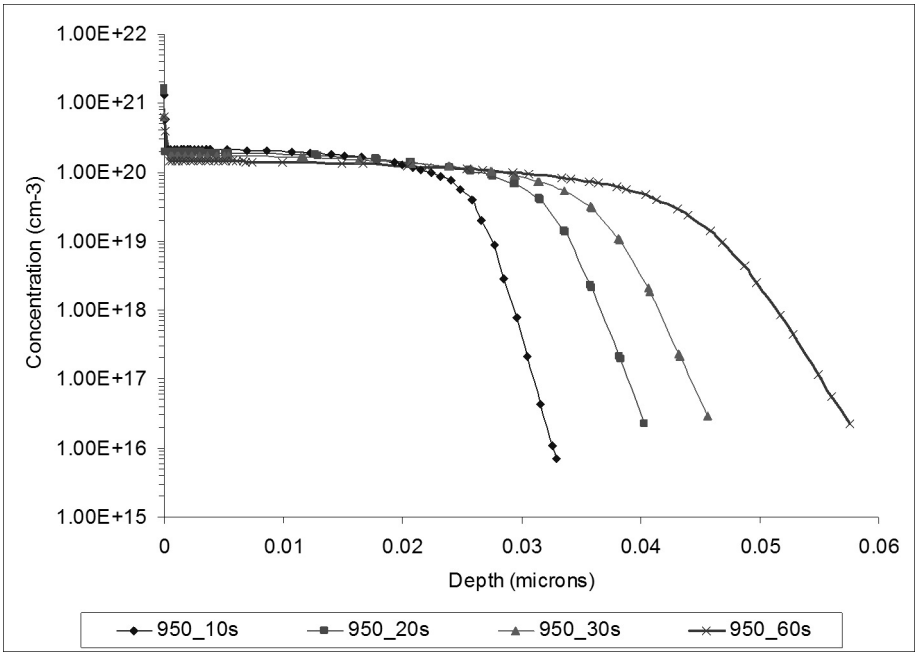

Fig. 9: Phosphorus profile for rapid thermal diffusion done at 950°C.

4. Conclusions

The process flow and the parameters used in this simulation can be applied to fabricate the actual source drain junction in laboratory since the dopant profiles are matched to the profiles obtained by the other researchers. The shallowest junction produced by rapid thermal diffusion technique. As expected, dopant diffuses to a deeper position by conventional furnace than rapid thermal annealing. This is caused by the longer processing duration for conventional furnace compared to rapid thermal system. Rapid thermal system

provides a highly controlled environment that is very difficult to achieve in conventional furnace.

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